SUBSTITUTE SPECIFICATION

TITLE OF THE INVENTION

Semiconductor device and its fabrication method

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

The present invention relates to a semiconductor device of an element using a ferroelectric thin film, particularly to a polarization inversion type non-volatile memory or a dynamic random access memory which is preferable to a large scale integrated circuit (LSI), and its fabrication method.

(2) DESCRIPTION OF THE PRIOR ART

There are ferroelectric substances which have extremely large relative dielectric constant, ranging from several hundreds to several thousands. Therefore, when a thin film made of these ferroelectric substances is used in a capacitor insulating film, a capacitor is provided which as a small area and a large capacitance preferable to a large scale integrated circuit (LSI). Further, a ferroelectric substance is provided with a capacitor dielectric and its direction can be inverted by an outside electric field and accordingly, a non-

volatile memory is provided by using the characteristic.

A memory is disclosed using a conventional ferroelectric substance in, for example, JP-A-5-90606. As shown by Fig. 22, a ferroelectric capacitor is formed by forming successively a lower Pt electrode 225, a ferroelectric thin film 226, an upper Pt electrode 227, and a Ti electrode 228 above an interlayer insulating film 224. Further, in the drawing, numeral 221 designates an isolation insulating film, numeral 222 designates a word line, numeral 223 designates an impurity diffused layer, and numeral 229 designates an aluminum wiring layer. However, according to the technology, the respective layers are fabricated by independent masks, and accordingly, this poses a problem of dimensional accuracy and matching accuracy. Hence, a structure has been proposed that is disclosed in JP-A-2-288368. That is, as shown by Fig. 23 this is a method of subjecting an upper electrode layer 238, a ferroelectric film 237, and a lower electrode layer 236 summarizingly to dry etching. However, by the summarizing fabrication, the leakage current is increased. Hence, a method is disclosed in JP-A-3-256358 in which, as shown by Fig. 24, only a lower electrode is fabricated, and a ferroelectric film and an upper electrode are not fabricated for each

cell, but are fabricated as a large pattern at an outer side of a memory mat or the like to thereby realize a highly integrated memory having a structure dispensing with matching allowance.

In the meantime, Fig. 25 shows a structure of another conventional memory cell disclosed in JP-A-7-14993. Although, according to the structure, only a lower electrode is finely fabricated and a ferroelectric film and an upper electrode are not fabricated for each cell, there is a feature in which an adhesion layer 251 is interposed between an interlayer insulating film and a capacitor insulating film. The article also describes that, as the adhesion layer, a layer of TiO_2, ZrO_2, Ta_2O_5 Si_3N_4 or the like is effective.

Further, as another conventional memory cell structure, a structure has been disclosed in JP-A-7-169854 in which, as shown by Fig. 26, a lower electrode and a dif fusion barrier layer are embedded in a reaction barrier film. This structure is obtained by the following process. First, an interlayer insulating film 248 and a polycrystal silicon film 246 are formed, thereafter, a titanium film 261 is formed, and, successively, a diffusion barrier layer 249 and a lower electrode 251 are formed. Thereafter, a ferroelectric film 252 is formed. In piling up the ferroelectric film 252,

the titanium film is oxidized and the TiO_2 film 261 of a reaction barrier layer is formed.

SUMMARY OF THE INVENTION

When lead zirconate titanate (PZT) is used in a capacitor insulating film in the above-described method disclosed in JP-A-3-256358, according to an investigation conducted by the inventors, at a portion where PZT and a silicon oxide film, which is an interlayer insulating film are brought into direct contact with each other, a reaction is caused therebetween. The reaction is caused even at the low temperature of about 500 °C, and particularly when PZT is formed at temperatures equal to or higher than 700 °C, the silicon oxide layer completely reacts with PZT and a melted state is brought about. It becomes apparent that this phenomenon is caused by lead, which is a major constituent element of PZT.

Further, in respect of the above-described method disclosed in JP-A-7-14993, according to an investigation conducted by the inventors, it has been found that although Si_3N_4 in the adhesion layer reacts with PZT, similar to the silicon oxide film, when TiO_2, ZrO_2, Ta_2O_5 is used for the adhesion layer, the adhesion layer serves as a reaction barrier layer between PZT and the silicon oxide film, and

therefore, the above-described problem of the reaction between PZT and the silicon oxide film can be resolved. However, according to the structure, it has been clearly found that since side faces of a diffusion barrier layer 249 disposed below a lower electrode are exposed, when the PZT film is formed by the CVD process or the like, necessitating a heated oxidizing atmosphere in the film forming operation, there poses a problem in which the diffusion barrier layer 249 is oxidized and the film is exfoliated. It has been found that, even in the case of using a sol-gel process, a sputtering process, a vapor deposition process or the like, a similar problem is posed in which, during the process of carrying out the heat treatment of crystallization, the diffusion barrier layer 249 is oxidized. It seems that although a metal nitride of TiN, (Ti, Al)N, WN, or the like is widely used in the diffusion barrier layer 249 and when the metal nitride is oxidized, nitrogen is discharged and therefore, the exfoliation of the film formed thereon becomes significant.

In the meantime, according to the method disclosed in JP-A-7-169854, when Ti is oxidized, the volume is expanded and exfoliation of the ferroelectric film is brought about.

It is an object of the present invention to achieve a semiconductor device which prevents a reaction between a ferroelectric film and an insulating film, and which also prevents film exfoliation and its fabrication method.

The above-described object is achieved by constituting a semiconductor device in which a reaction barrier film is provided between a ferroelectric film and an interlayer insulating film. Side faces of the diffusion barrier film and the ferroelectric film are not brought into contact with each other, and the side walls of a lower electrode and the ferroelectric film are brought into contact with each other.

By constructing the above-described constitution, in the case in which, for example, TiO_2 is used for the reaction barrier film, when the film thickness is equal to or larger than 2 nm, it is effective in preventing a reaction between a silicon-species interlayer insulating film and lead included in a capacitor insulating film, even in a rapid heat treatment at about 700 °C which is needed in crystallizing a PZT film. Further, only the diffusion barrier film is embedded into the reaction barrier film, and, therefore, the side walls of the lower electrode can be utilized as a capacitor,

which is particularly effective in the case of applying to the DRAM.

Further, the above-described object is achieved by embedding the diffusion barrier film in the interlayer insulating film as plugs and by interposing the reaction barrier film between the capacitor insulating film and the interlayer insulating film. Also in this structure, a lower electrode is formed on the plug, and accordingly, a ferroelectric film is installed from a side face to an upper face of the lower electrode. The side walls of the lower electrode can also be utilized as a capacitor, which is particularly effective in the case of using the invention in a DRAM.

Further, the above-described object is achieved by forming the reaction barrier film in a manner such that it functions to prevent a reaction on the interlayer insulating film, and, thereafter, forming the diffusion barrier film and the ferroelectric film. Before forming the diffusion barrier film and the ferroelectric film, the reaction barrier film is formed previously as an oxide, and, therefore, even when the reaction barrier film per se is formed by oxidizing a metal film, there poses no problem of exfoliation by volume expansion or the like.

Although the case in which PZT is used for the capacitor insulating film has been described, a similar effect is observed even in the case of using lead-species ferroelectric substance other than PZT or a Bi-species lamellar ferroelectric substance such as $Bi_4Ti_3O_{12}$, $Sr_2Bi_2Ta_5O_9$ or the like. When using a Bi-species lamellar ferroelectric substance, generally, mutual diffusion with an interlayer insulating film becomes significant because the crystallizing temperature is higher than that of the Pb-species ferroelectric substance, and, accordingly, the use of a reaction barrier film becomes a necessity.

Further, it has been considered conventionally that in the case of a dielectric substance which does not include lead or bismuth, for example, strontium barium titanate (BST), the reaction with the silicon oxide film constituting the matrix of the lower electrode is not significant, and poses no serious problem. However, according to an investigation conducted by the inventors, it has been found that although the diffusion coefficient is smaller than that of Pb or Bi, Ba or Sr also diffuses into the SiO_2, matrix. Therefore, it is found that the significance of installing the reaction barrier film is great, even in the case of using a film of BST-species.

The foregoing and other object, advantages, manner of operation, and novel features of the present invention will be understood from the following detailed description when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view of a semiconductor device according to a First Embodiment of the present invention;

Fig. 2 is a first sectional view showing a fabrication step of a memory cell using the present invention;

Fig. 3 is a second sectional view showing a step of the First Embodiment according to the present invention;

Fig. 4 is a third sectional view showing a step of the First Embodiment according to the present invention;

Fig. 5 is a fourth sectional view showing a step of the First Embodiment according to the present invention;

Fig. 6 is a fifth sectional view showing a step of the First Embodiment according to the present invention;

Fig. 7 is a sixth sectional view showing a step of the First Embodiment according to the present invention;

Fig. 8 is a sectional view of a semiconductor device according to a Second Embodiment of the present invention;

Fig. 9 is a first sectional view showing a fabrication step of a memory cell according to the Second Embodiment using the present invention;

Fig. 10 is a second sectional view showing a step of the Second Embodiment of the present invention;

Fig. 11 is a third sectional view showing a step of the Second Embodiment of the present invention;

Fig. 12 is a sectional view of essential portions of respective portions of a memory cell array portion and a peripheral circuit contiguous thereto according to the present invention;

Fig. 13 is a plane view of respective portions of the memory cell and the peripheral circuit according to the present invention;

Fig. 14 is a circuit diagram showing respective portions of the memory cell and the peripheral circuit according to the present invention:

Fig. 15 is a first sectional view showing a fabrication step of a memory cell according to a Third Embodiment using the present invention;

Fig. 16 is a second sectional view showing a fabrication step of a memory cell according to the Third Embodiment using the present invention;

Fig. 17 is a third sectional view showing a fabrication step of a memory cell according to the Third Embodiment using the present invention;

Fig. 18 is a fourth sectional view showing a fabrication step of a memory cell according to the Third Embodiment using the present invention;

Fig. 19 is a fifth sectional view showing a fabrication step of a memory cell according to the Third Embodiment using the present invention;

Fig. 20 is a sixth sectional view showing a fabrication step of a memory cell according to the Third Embodiment using the present invention;

Fig. 21 is a sectional view of a semiconductor device according to the Third Embodiment of the present invention;

Fig. 22 is a sectional view of a semiconductor device according to conventional technology;

Fig. 23 is a sectional view of a semiconductor device according to conventional technology;

Fig. 24 is a sectional view of a semiconductor device according to conventional technology;

Fig. 25 is a sectional view of a semiconductor device according to conventional technology; and

Fig. 26 is a sectional view of a semiconductor device according to conventional technology.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(First Embodiment)

An explanation will be given of a preferred embodiment of the present invention with reference to Fig. 1. In accordance with the present invention, a diffusion barrier layer 43 formed by a known method is embedded in a reaction barrier layer 44 above an element layer including transistors formed by a publicly-known method. Above these, a lower electrode is formed and fabricated in a desired shape, thereafter, a ferroelectric thin film 71 including lead and an upper electrode 72 are formed.

According to the structure, the ferroelectric thin film 71 and the upper electrode 72 are not separated into patterns in correspondence with respective memory cells, but are continuously present over a plurality of memory cells. With respect of the two layers, only the minimum fabrication necessary for operating a storage device (for example, a portion for separating a memory cell region from another region) is carried out, and the

requirement for fabrication accuracy is considerably alleviated.

Further, the diffusion barrier layer 51 is embedded in the reaction barrier layer 43 and is not oxidized in the crystallization heat treatment of the ferroelectric thin film 71.

Fig. 2 through Fig. 6 show an embodiment of fabricating a memory cell by using the present invention. First, as shown in Fig. 2, a switch transistor is formed by a conventional step of forming MOSFET. N-type impurity (phosphor) diffusion layers 25 and 26 are formed in a p-type semiconductor substrate 21, and inter-element isolation oxide films 22, a gate oxide film 23, a word line 24, and an insulating film 27 are formed. Successively, an SiO_2 layer 28 having a thickness of 600 nm is piled up by a CVD process over an entire surface by using a publicly-known CVD process, ref lowed at 850 °C, and, thereafter, etched back by 300 nm to thereby alleviate a stepped difference caused by the word line.

Next, a portion 25, where a bit line is brought into contact with the n-type diffusion layer at the surface of the substrate, is opened by using a known photolithography process and dry etching process (Fig. 3) Next, a bit line 31 is formed. For the material of the bit line, a laminated layer film

of silicide of metal and polycrystal silicon is used. Fabrication is carried out by using a publicly-known photolithography process and dry etching process to thereby constitute the bit line in a desired pattern. Next, an insulating film 32 of a silicon oxide film-species such as BPSG is piled up and flattened. The insulating film 32 needs to be provided with a film thickness sufficient for flattening the substrate surface. According to the embodiment, the film thickness of the insulating film 32 is determined to be 600 nm, and a method of flattening by known chemical and mechanical polishing process is used. Next, a reaction barrier layer 33 is formed on the interlayer insulating film. In forming the reaction barrier layer, a method of piling up a TiO_2 film to a thickness of 50 nm by a reactive sputtering method and a method of piling up a Ti film and thereafter oxidizing Ti by heat treatment at 750 °C for 30 minutes in an oxygen atmosphere and an excellent result is obtained by both of them.

Next, as shown in Fig. 4, by using a known photolithography process and dry etching process, a memory contact hole 41, by which a storage capacity portion is brought into contact with the substrate, is opened. A polycrystal silicon layer 42 is deposited to a thickness of 350 nm on the insulating

film 32 and on the inner side of the contact hole by using a CVD process. Next, the polycrystal silicon layer 42 is etched back by an amount of the film thickness by using a dry etching process to thereby fill the contact hole. Further, overetching in correspondence with a film thickness of 50 nm is added, and a structure in which the surface of the polycrystal silicon layer sinks into the hole is constructed. Next, a TiN layer having a thickness of 100 nm is formed by using a sputtering process as a diffusion barrier layer 51, and is flattened by a CMP process to thereby embed the TiN layer in the contact hole. In this way, the embedded diffusion barrier layer of Fig. 5 is formed.

Next, a Pt film 61 having a thickness of 100 nm is coated as a matrix electrode 61 by a sputtering process (Fig. 6), and, successively, a tungsten layer 62 having a thickness of 100 nm is coated as a mask for fabricating the Pt layer. A pattern is transcribed on the tungsten layer 62 by a dry etching process, using SF_6 with a photoresist 63 as a mask. After removing the photoresist 63, the lower electrode 61 is patterned by a sputter etching process, using the tungsten layer 62 as the mask.

After removing the tungsten mask, a ferroelectric thin film 71 is formed (Fig. 7). According to the embodiment, by a reactive

evaporation process, a thin film of lead titanate zirconate ($Pb(Zr_{0.5}Ti_{0.5})O_3$) having a thickness of about 100 nm is formed, and, thereafter, subjected to heat treatment at 650 °C for 30 seconds to thereby crystallize the film. In forming the ferroelectric thin film, a reactive sputtering method or a CVD process may also be used. Next, a Pt film 72 having a thickness of 50 nm is coated as an upper electrode by a sputtering process. Thereafter, an interlayer insulating film and wirings are provided to thereby complete the memory cell of Fig. 1.

(Second Embodiment)

Fig. 8 shows an embodiment in which the present invention is used in DRAM. According to the embodiment, a capacitor lower electrode is thickened and its side walls are utilized to thereby increase the electrostatic capacitance of the capacitor.

An explanation will be given of a method of fabricating a memory cell by using the present invention, with reference to Fig. 9 through Fig. 11. Fabrication steps up to forming the embedded diffusion barrier layer, as shown in Fig. 5, are the same as those in the First Embodiment.

As shown in Fig. 9, a matrix electrode 91 is formed by a sputtering process. According to the embodiment, as the matrix electrode, an Ru film

having a thickness of 400 nm is used. The lower electrode 91 is fabricated by a dry etching process by using an SiO_2 layer as a mask, and the SiO_2 mask is removed to thereby provide a structure shown by Fig. 10.

Next, a BST film 111 is piled up by 30 nm by using an MOCVD process, as shown in Fig. 11. Thereafter, an upper electrode is formed and wirings are provided to thereby complete the memory cell of Fig. 8.

(Third Embodiment)

Next, an explanation will be given with reference to Figs. 15 through 21 of an embodiment of the present invention in which a matching allowance between a lower electrode and a contact plug is dispensed with, and a fine memory cell suitable for high integration can be realized by self-adjustingly forming a reaction barrier layer to the lower electrode of a capacitor.

First, as shown in Fig. 15, the inter-element isolation insulating film 22 and the gate oxide film 23 are formed on the p-type semiconductor substrate 21. A polycrystal silicon layer having a thickness of 60 nm, and the bit line 24 comprising tungsten silicide having a thickness of 60 nm, and an Si_3N_4 layer 151 having a thickness of 200 nm are successively piled up and fabricated by using a

known photolithography process and dry etching process to thereby constitute a desired pattern of a word line for forming a gate electrode. The n-type impurity (phosphor) diffusion layers 25 and 26 are formed by ion implantation with the word line as a mask. An Si_3N_4 layer having a thickness of 80 nm is coated by a CVD process and fabricated by an anisotropic etching method to thereby form insulating film layers 152 at side walls of the word line.

Next, as shown by Fig. 16, an SiO_2 layer 161 having a thickness of 300 nm is piled up by using a known CVD process, and, thereafter is flattened by a CMP process. Next, an Si_3N_4 layer 162 having a thickness of 40 nm is piled up by using a publicly-known CVD process.

By using a known photolithography process and dry etching process, contact holes are perforated from the portion 25 where the bit line is brought into contact with the n-type diffusion layer at the surface of the substrate and from the portion 26 where the store electrode is brought into contact with the n-type dif fusion layer at the surface of the substrate leading to a peripheral circuit (Fig. 17). By a CVD process, a TiN layer having a thickness of 100 nm is piled up and the TIN layers 181 are embedded into the contact holes by a CMP

process. Next, a first wiring layer is formed, as shown in Fig. 18. For material, a laminated layer film 182 of W/TiN/Ti is used. The laminated film of W/TiN/Ti is piled up by a sputtering process, an SiO_2 layer 183 having a thickness of 50 nm is piled up thereon, and, thereafter, is fabricated by using a known photolithography process and dry etching process to thereby constitute the first wiring layer in a desired pattern. The first wiring layer is used for wiring the bit line and a peripheral circuit. An SiO_2, layer having a film thickness of 50 nm is piled up by a CVD process and etched back by a dry etching process, and side wall spacers 184 are formed at side wall portions of the first wiring layer to thereby insulate the first wiring layer.

Next, an insulating film 191 of a silicon oxide film-species such as BPSG is piled up and flattened. According to the embodiment, the film thickness of the insulating film 191 is determined to be 250, nm and the insulating film 191 is flattened by a CMP process. By using a known photolithography process and dry etching process, a memory portion contact hole is perforated for connecting a store capacitance portion and a dif fusion layer. At the same time, there are perforated contact holes for connecting the first wiring layer and a second wiring layer. A TiN layer

having a thickness of 100 nm is piled up by a CVD process, and a TiN layer 192 is embedded into the contact holes by a CMP process.

Next, as shown in Fig. 19, a Ti film 193 having a film thickness of 2 nm and a Pt film 194 having a film thickness of 300 nm are successively piled up by a sputtering process, and successively, a tungsten layer 195 is piled up by 300 nm. By a dry etching process using a SF, with a photoresist as a mask, a pattern is transcribed on the tungsten layer 195. After removing the photoresist, a structure shown in Fig. 20 is provided by fabricating the lower electrode 194 by a sputter etching process, using the tungsten layer as a mask. By adding oxygen to Ar in sputter etching, the selectivity between Pt and Ti can be promoted sufficiently. After the etching operation, by rapid a heat treatment at 700 °C for 5 seconds in an oxygen atmosphere, the Ti film 193 disposed below the Pt film 194 forms an alloy with Pt and vanishes. Further, a reaction barrier film 211 is self-adjustingly formed only on the interlayer insulating film 191, which is exposed at a surrounding area of the lower electrode.

Next, as shown in Fig. 21, a strontium barium titanate layer 211 having a thickness of 20 nm and a ruthenium dioxide layer 212 having a thickness of 20

nm are successively piled up by an MOCVD process. At the portions where the plate electrode is not necessary outside of a memory mat, the ruthenium dioxide layer and the strontium barium titanate layer are removed with a photoresist as a mask, and, thereafter, wiring is carried out to thereby complete a memory cell. Although, according to the embodiment, Pt is used as the material of the lower electrode, Ru or Ir may naturally be used.

(Fourth Embodiment)

Fig. 12 is a sectional view showing essential portions of respective portions of a memory cell array portion, and a peripheral circuit contiguous thereto. Fig. 13 is a plane view of respective portions of a memory cell according to the present invention and a peripheral circuit, and Fig. 14 is a circuit diagram showing respective portions of the memory cell according to the present invention and the peripheral circuit. Fig. 12 is a sectional view taken along a line X-X' of Fig. 13. Fig. 12 shows MISFET Q_t for selecting a memory cell, and MISFETS of a peripheral circuit attached with notations Q_{shr}, Q_p, and Q_n in Fig. 13 and Fig. 14. Notation Q_{shr} designates shared MISFET for separating a memory cell portion of DRAM and a sense amplifier of a peripheral circuit portion. Notation Q_p designates a p-channel MISFET, notation Q_n designates an n-channel

MISFET, and a sense amplifier portion is constituted by a flip flop circuit comprising two of Q_p and two of Q_n.

An explanation will be given of a reading operation when a memory according to the present invention is used as a DRAM in reference to the circuit diagram shown in Fig. 14. The potential of a plate electrode PL1 of a capacitor is always fixed at vcc/2. In the meantime, at the storage node SN1 of the capacitor, volatile information Vcc or 0 is held. The potential of a bit line pair BL1 and BL1LB is held at Vcc/2 immediately before a reading or rewriting operation. The bit line pair is connected with a sense amplifier SA for detecting amplified stored information. In order to detect the storage voltage of the storage node SN1, the potential of a precharge control line PCL1 is lowered from Vcc to 0 and a bit line is brought into a floating state having a potential of Vcc/2. At the same time, the shared MISFET Q_{shr} is turned ON. Next, the potential of a word line WL1 is elevated from 0 to Vch. In this case, Vch is a potential that is higher than Vcc by at least the threshold voltage of transistor. As a result, when the potential of the store node is Vcc, the potential of the bit line BL1 becomes slightly higher than the potential of BL1B, that is, Vcc/2. On the other

hand, when it is 0, the potential of BL1 becomes slightly lower than that of BL1B. By detecting and amplifying the potential difference by the sense amplifier SA1, the potential of BL1 coincides with the potential of the store node to be Vcc or 0. The potential of BL1B becomes opposed to that of BL1. Further, in order to operate the sense amplifier, a p-channel transistor control line CSP for the sense amplifier and an n-channel transistor control line CSN of the sense amplifier may respectively be set to Vcc and 0. By the above operation, the information from all of the memory cells connected to the selected word line WL1 is read by respectively connected bit lines. In order to read the information of one of the memory cells to the outside of the memory device selectively via an IO line, the potential of the sense amplifier selecting line CSLL may be changed from 0 to Vch, and the desired bit line may be connected to the IO line. In order to finish the reading operation, when the potential of CSLL is returned from Vch to 0, and, thereafter, the word line WL1 is returned to 0, the storage node SN1 is electrically separated from the bit line in a state in which information is rewritten. When PCL1 is returned to Vcc and CSP and CSN are returned respectively to 0 and Vcc, there is

brought about a state existing before the reading operation, and the reading operation is finished.

Next, an explanation will be given of a reading and writing procedure based on JP-A-7-21784, when the memory of the present invention is used as ferroelectric involatile memory.

First, it is to be noted that the reading operation is the same as in the above-described case of DRAM.

In rewriting information in the ferroelectric involatile memory, polarization inversion of a ferroelectric film is carried out along with potential inversion of the store node SN1. The rewriting operation is the same as the reading operation until the signal line PCL1 is lowered from Vch to 0 and the sense amplifier is operated. Next, in order to write rewrite information prepared at the IO line to the memory cell, the signal line CSLL is elevated from 0 to Vch. As a result, potentials of the bit line pair BL1 and BL1B are inverted. Since the word line WL1 is brought into an activated state, in accordance with the potential inversion of the bit line, the store node potential of the desired memory cell and the polarization direction of the ferroelectric film are inverted. In this way, after rewriting information, the rewiring operation is finished by a procedure similar to that

of the reading operation. According to the reading and writing procedure, volatile information and involatile information are always rewritten coincidently, and, therefore, even when the power source is turned OFF, the information does not vanish.

Next, an explanation will be given of the operation of converting involatile information to volatile information when the power source is turned ON in the ferroelectric involatile memory. Before inputting the power source, all potential is at OV. In accordance with the power source ON, the plate PL1 is initialized to Vcc/2, and the signal lines CSP and CSN of the sense amplifier are initialized to 0 and Vcc. Further, the potential of the signal line PCL rises from 0 to Vcc, and, as a result, the potential of the bit line pair BL1 and BL1B is precharged to Vcc/2. At this time, the potential of the word line maintains OV and the store node SN1 is brought into a floating state such that the polarization direction of the ferroelectric film is not destroyed when the voltage of the plate is elevated. When the potentials of the plate PL1 and the bit line pair BL1 and BL1B are firmly stabilized to a potential of Vcc/2, the word lines WL are successively activated, and the store node SN1 is set to a potential of Vcc/2, the same as that of the

plate PL1 to thereby further stabilize the holding of polarization information. Successive to the above-described initializing an operation, the operation shifts to an operation of converting from involatile information to volatile information. First, the potential of PCL1 is set to OV, in a state in which all of the word lines are at OV, and the bit line is brought into a floating state. Next, the bit line is precharged to OV and is again brought into the floating state. Thereafter, when the word line WL1 is activated, current flows from the store node SN1 to the bit line, and the potential of the bit line is elevated. The amount of elevation is dependent on the polarization direction of the ferroelectric film. That is, even after elevating the potential of the bit line, the plate potential is higher, and, therefore, the polarization direction is aligned to one direction. The effective capacitance of the ferroelectric capacitor is larger in the case accompanied by inversion of polarization by activating the word line than in the case that is not accompanied by the inversion. As a result, the amount of potential elevation of the bit line is also larger. A dummy cell is installed for producing an intermediary value of the amount of potential elevation of the bit line in correspondence with the two polarization

states in the compensating bit line BL1B, and the potential difference of the bit line pair BL1 and BL1B is detected and amplified by the sense amplifier SA1. By operating the sense amplifier, the bit line potential is charged to Vcc or 0,and, as a result, the storage node SN1 is written with volatile information. Finally, the word line is deactivated, and, thereafter, the bit line potential is returned to Vcc/2 to thereby finish the series of operations. When the above-described operation is successively carried out for the respective word lines, the operation of converting from involatile information to volatile information is finished. According to the procedure, inversion of polarization of the ferroelectric film accompanied by an information reading operation can be executed only when the power source is inputted, and, accordingly, the deterioration of the ferroelectric film can be reduced. Further, there is no reduction in the reading speed caused by the time period required for the polarization inversion during normal use. Further, information at the time point when the power source is turned OFF is stored and the information can be revived when the power source is successively turned ON.

Although according to the above described embodiments, an explanation has been given by using

a dielectric substance including lead as the ferroelectric material, in the case of a material reacting with silicon oxide at the temperature at which the ferroelectric film is formed, the present invention is effectively naturally applicable. Especially in the case of a material including bismuth, the present invention is particularly useful since a violent reaction is caused, as in the case of lead. That is, the preferred dielectric material for use in the present invention is an oxide dielectric including an element selected from lead and bismuth. As materials corresponding thereto other than PZT shown in the above-described examples, there are lead titanate ($PbTiO_3$) lead barium zirconate titanate ((Ba, Pb) (Zr, Ti)O_3), barium lead niobate ((Ba, Pb)Nb_2O_6, strontium bismuth tantalite ($SrBi_2Ta_2O_9$), bismuth titanate ($Bi_4Ti_3O_{12}$), and barium strontium titanate zirconate (Ba, Sr)(Zr, Ti)O_3 . The present invention is applicable to all dielectric substances having these as a basic structure. That is, it may be an oxide described in the form of (A_1A_2..) (B_1B_2 ..) OX (A_1 = Pb, Bi; A_2 = Ca, Sr, Cd, Ba, La, Tℓ, Na, K; B_1, B_2.. = Ta, Ti, Zr, Hf, Fe, Nb, Sn, U, Aℓ, Mn, W, Yb, Sc, U. In, Sb, Co, Zn, Li, Mo, Ni, Co). Further, the present invention includes a case in which other elements

are mixed with a material having major components of these.

Although as the reaction barrier layer, the titanium dioxide film is used in the above-described embodiments, a film having a major component of an oxide of elements selected from the above-described elements as B_1 and B_2, that is, Ta, Ti, Zr, Hf, Fe, Nb, Sn, U, Aℓ, Mn, W, Yb, Sc, U. In, Sb, Co, Zn, Li, Mo Ni and Co is also effective. Particularly, titanium oxide, aluminum, or bismuth silicate are effective.

Although according to the above-described embodiments, platinum is used as a material of an electrode, the electrode material can be implemented even with metals having major components of metals selected from Ru, Ir, Pd, Ni, Pt, and alloys of these, or oxides of elements selected from V, Cr, Fe, Ru, In, Sn, Re, Ir, Pt, Cu, and Pd.

Further, a diffusion barrier conductive layer may use a material selected from Ti, Ta, TiN, Al_xTi_{1-x},N, and WN, or a plurality thereof by laminating them.

Although according to the embodiments, as a process of forming the reaction barrier layer, a sputtering process and thermal oxidation of a metal thin film are shown, other than a reactive sputtering in an oxygen including atmosphere, a thin

film formed by a CVD process, or a sol/gel coating process, is also applicable.

According to the present invention, even when a dielectric substance including lead is used as a capacitor insulating film, a reaction with an interlayer insulating film or a diffusion barrier layer can be restrained, and therefore, a highly integrated semiconductor storage device can be realized.